Received from < 518 449 0047 > at 1/28/03 5:57:25 PM [Eastern Standard Time]

to a depth (h), and wherein the metal silicide includes a substantially planar surface that is higher than the larger isolation layer.

REMARKS

The status of the application is as follows. Claims 1-9 were presented for prosecution and stand rejected. Claims 1-4, and 6-8 were rejected under 35 USC 102(b) as allegedly being anticipated by Kawaguchi (U.S. 5,739,573) "Kawaguchi." Claims 1, 5-6, and 9 were rejected under 35 USC 103(a) as allegedly being unpatentable over Lur et al. (U.S. 6,013,569) "Lur" in view of Kawaguchi. Claims 1 and 6 have been amended herein. No new matter is believed added.

Applicants respectfully traverse the finding that independent claim 1 is anticipated by Kawaguchi. In particular, Kawaguchi fails to teach, *inter alia*, "a depth of the trench, measured from a top of the larger isolation layer down to the smaller isolation layer, [that] is maximally half the height of the larger isolation area." Rather, as can be seen in Figure 5C of Kawaguchi, the trench depth, **measured from a top of the larger isolation layer down to the smaller isolation layer,** is greater than half the height of the larger isolation layer. Accordingly, Kawaguchi fails to teach each and every claim element of claim 1.

Applicants also traverse the finding that independent claim 1 is unpatentable over Lur in view of Kawaguchi. As admitted in the Office Action, Lur fails to describe "a smaller isolation layer (402) that is formed by depositing an oxide layer over and around the polysilicon region in a single step." Rather, Lur describes a method in which "a

JAN.28'2003 19:06 518 449 0047 HOFFMAN WARNICK D ALESSANRO LLC #4790 P.004/009

Received from < 518 449 0047 > at 1/28/03 5:57:25 PM [Eastern Standard Time]

sacrificial material 56 is first provided over the polysilicon layer 56," later followed by a thermal oxidation process in order "to grow a thin liner oxide layer 58 over the sides," see Lur, column 7, lines 5-50. To address this deficiency, the Office Action states that Kawaguchi teaches depositing an oxide layer over and around the polysilicon region in a single step, and therefore it would have been obvious to modify Lur to include the teachings of Kawaguchi.

Applicants respectfully disagree. A careful reading of Lur discloses that "a layer of sacrificial material 56 is provided" which "has a variety of different preferred uses in the embodiments of the present invention." See column 7, lines 5-24, which describe the motivation and advantages for utilizing the sacrificial material 56. Because the sacrificial material is used, the teachings of Lur **require** a two-step deposition process. In sharp contrast to the teachings of Lur, the Examiner is suggesting that one skilled in the art would eliminate the use of the sacrificial material (and all of its benefits) as taught by Lur to arrive at the single step process claimed by Applicants. Clearly, Lur provides no motivation for eliminating the use of the sacrificial material, and there is no suggestion or teaching in Lur that would lead one of ordinary skill in the art to utilize a one step process in which a sacrificial material was not present. Rather, the teachings of Lur explicitly require a two-step deposition process in order to obtain the preferred embodiments of the invention. Thus, Lur teaches away from using a single step deposition process.

Accordingly, because Lur provides no motivation, teaching or suggestion of using a single step deposition process, as recited in claim 1, Applicants respectfully submit that claim 1, and the claims that depend therefrom, are not obvious in view of the cited art.

JAN.28'2003 19:06 518 449 0047 HOFFMAN WARNICK D ALESSANRO LLC #4790 P.005/009

Received from <518 449 0047> at 1/28/03 5:57:25 PM [Eastern Standard Time]

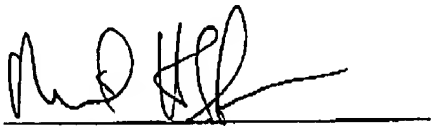
Finally, Applicants further traverse the finding that claim 6 is anticipated by Kawaguchi, or is unpatentable over Lur in view of Kawaguchi. Both Kawaguchi and Lur fail to teach, *inter alia*, an integrated circuit, "wherein the metal silicide includes a substantially planar surface that is **higher** than the larger isolation layer." A careful examination of both Kawaguchi and Lur shows a metal silicide surface that is **lower than** the larger isolation layer (see Figures 5F and 9 of the respective patents). Moreover, the silicide surface of Lur is not planar, but rather is concave in shape. In response to similar arguments made in the prior amendment dated September 27, 2002, the Examiner states "Kawaguchi teaches an integrated circuit comprising a metal silicide in the upper part of the polysilicon region." This fact, whether true or not, fails to address the recited claim feature -- namely, a planar surface that is **higher** than the larger isolation layer. Accordingly, because the two references fail to teach each and every claim element of claim 6, Applicants respectfully submit that claim 6, and the claims that depend therefrom are in condition for allowance.

JAN.28'2003 19:07 518 449 0047 HOFFMAN WARNICK D ALESSANRO LLC #4790 P.006/009

Received from <518 449 0047> at 1/28/03 5:57:25 PM [Eastern Standard Time]

Applicants submit that all claims are therefore in condition for allowance. If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,



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JAN.28'2003 19:07 518 449 0047 HOFFMAN WARNICK D ALESSANRO LLC #4790 P.007/009

Received from < 518 449 0047 > at 1/28/03 5:57:25 PM [Eastern Standard Time]

SEPARATE MARKUP SHEET

In the Claims

1. (TWICE AMENDED) A method of manufacturing an integrated circuit, which method includes a stage wherein lateral isolation regions (spacers) are formed at the sides of a projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer (402) that is formed by depositing an oxide layer over and around the polysilicon region in a single step, which is in contact with said projecting region (2), and of a larger isolation layer, which method also includes a silicidation process to which the upper part of the polysilicon region is subjected, which silicidation process includes the deposition on said upper part of a metal layer which is capable of forming a metal silicide (5) with the silicon, characterized in that the silicidation process includes, prior to the deposition of said metal layer, an etch step to which at least the vertical portion of the smaller isolation layer (402) is subjected so as to form a trench (TR) between the larger isolation layer (411) of each lateral isolation region and the corresponding side (F) of the polysilicon region (2), wherein a depth of the trench, measured from a top of the larger isolation layer down to the smaller isolation layer, [comprises a depth that] is maximally half the height of the larger isolation area, and in that the deposition of the metal layer is a directional deposition.

6. (TWICE AMENDED) An integrated circuit comprising lateral isolation regions formed at the sides of a least one projecting region of polysilicon so as to be in contact therewith, each lateral isolation region being composed of a smaller isolation layer (402),

JAN.28'2003 19:07 518 449 0047 HOFFMAN WARNICK D ALESSANDRO LLC #4790 P.008/009

Received from < 518 449 0047 > at 1/28/03 5:57:25 PM [Eastern Standard Time]

contacting said projecting region (2), and a larger isolation layer (411), and comprising a zone (5) including a metal silicide situated in the upper part of the polysilicon region (2), characterized in that each lateral isolation region comprises a vertical trench (TR) made in the smaller isolation layer (402) between the larger isolation layer (411) and the corresponding side (F) of the projecting region (2), said trench (TR) extending from the top of the larger isolation layer (411) of the corresponding lateral isolation region down to a depth (h), and wherein the metal silicide includes a substantially planar surface that is [above] higher than the larger isolation layer.

JAN.28'2003 19:07 518 449 0047 HOFFMAN WARNICK D ALESSANRO LLC #4790 P.009/009